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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,387	07/01/2003	Jing-Rung Wang	MR3003-47	9382

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EXAMINER	
BRITT, CYNTHIA H	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 02/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,387	WANG, JING-RUNG	
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-12 are presented for examination.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

The drawings received on July 1, 2003 are acceptable.

Specification

The disclosure is objected to because of the following informalities: The examiner would like to point out that this application should be proofread and corrected for the numerous grammatical errors. Example Background page 1 paragraph 1 line 3 'existed' should be 'existing'. Line 6 same paragraph 'may' should be 'has' (this is the background of the invention and past tense is appropriate).

Appropriate correction is required.

Claim Objections

Claim 5 is objected to because of the following informalities: "providing at least one sets..." in lines 3-4 should read "providing at least one sets...". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims rejected under 35 U.S.C. 103(a) as being unpatentable over Merkin et al. U.S. Patent No. 5,634,137 in view of Delp et al. U.S. Patent No. 6,601,200.

As per claim 1, Merkin et al. substantially teaches the claimed method for testing chip configuration settings, by providing a main board including a chip to be tested (column 1 lines 48-52) providing a BIOS program starting power; performing a power on self test (column 1 lines 29-35) loading said BIOS program; (column 1 lines 48-55, Figure 5). Not disclosed by Merkin is the configuration test process.

However, in an analogous art, Delp et al. teaches testing of chip configuration (column 1 lines 36-44 column 7 lines 55-67, column 8 line 56 through column 9 line 8).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the configuration test of Delp et al. with the BIOS of Merkin et al. One would have been motivated to use this combination in order to confirm proper operation of the IC in the board environment.

As per claim 2, Delp et al. teach a configuration test process including providing a test data, providing an expected result data and comparing the two (column 6 lines 55-65).

As per claim 3, Delp et al. teach recording said comparison result. (Figure 9 element 940)

As per claim 4, Delp et al. teach generating a difference report. (Column 5 lines 33-47)

As per claim 5, Delp et al. teach providing test data; providing expected result data corresponding to said test data; inputting said test data; enabling a register woth reference to test data; obtaining corresponding result data after operating of said chip in accordance with said test data; and comparing said obtained result data with said corresponding expected result data. (Figures 3, 9, and 12)

As per claims 6-12, generating data tables and error (difference reports), in table form and various other forms are well known in the art, and the prior art is replete with examples of such lists and tables. Note the lists of prior art references listed in conclusion. Delp et al teaches “When a chip under test receives a message on the

network to execute an operation, it performs the requested operation, and then reports the results." (Column 5 lines 6-8)

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,410,551 Edwards et al.

This patent teaches an error detecting system automatically detects the error and sends an error-condition report (Figure 2 and associated description) for reporting a difference between an expected value and an actual value.

U.S. Patent No. 4,9072,30 Heller et al.

This patent teaches functional testing of digital circuits applies digital patterns to circuit inputs and compares the circuit output to expected values. Another object of the invention is to automatically learn the differences between a particular component while in circuit and while out of circuit. The invention tests for these differences and modifies out-of-circuit models accordingly. Another object of the invention is to acquire and analyze test data. The invention stores test and repair data for historical and statistical purposes, and generates reports

U.S. Patent No. 5,369,647 Kreifels et al.

This patent also teaches a method of testing where actual data is compared to expected data and reports are generated.

"*Configuration Self-Test in FPGA-based Reconfigurable Systems*" by Quddus et al. IEEE International Symposium on Circuits and Systems, 1999. Publication Date: Jul 1999 Vol.1, pages 97-100 ISBN: 0-7803-5471-0 INSPEC Accession Number: 6382155

This paper teaches a FPGA-based reconfigurable system may contain boards of FPGAs which are reconfigured for different applications and must work correctly. This paper presents a novel approach for rapidly testing the configuration in the FPGAs each time the system is reconfigured. A low-cost configuration-dependent test method is used to detect faults in the circuit. The "original configuration" is modified by only changing the logic function of the CLBs to form "test configurations" that can be used to quickly test the circuit. The test procedure is rapid enough to be performed on the fly whenever the system is reconfigured.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2138